**Face-To-Face Student/Supervisor Meeting Record**

|  |  |  |  |
| --- | --- | --- | --- |
| **Project Title:** | Design and Implementation of a Multi-core Processor using FPGA | **Photo:** |  |
| **Student Name:** | Matteo Bovino | **Student ID:** | 8671055 |
| **Supervisor:** | Dr Server Kasap | **Student UID:** |  |
| **Supervisor UID:** |  | **Department:** | AAEEE |
| **Course Code:** | Electrical and Electronic Engineering | **Module Code:** | 306AAE |
| **Date Today:** | 05/02/2021 | **Time:** | 02:00 PM |

|  |  |
| --- | --- |
| **Current Progress and Issues:** | |
| *In this meeting we discussed about the current status of the project, areas to improve and timing requirements.*  *The supervisor reminded me about the priorities and deadlines associated with the final implementation. I showed my current work and what I developed since the last meeting and received feedback on it. I also cleared some of the doubts that I encountered while building parts of the single core processor. Multiple issues were analysed, e.g., the instruction/data memory and the hazard detection unit.* | |
| **Agreed Key Action Points:** | |
| *While discussing the current design we also set targets for the next meeting. The agreed goal is to develop the second core within this two-week period. Once all the functional parts of the design are achieved a simulation should be prepared in order to highlight the execution of basic instructions. To do so, I was prompted to shift my attention to broader design constraints and not to focus excessively on minor details. This recommendation is extremely important, especially due to the high number of details present in modern processor design.* | |
| **Date and Time of next meeting:** | 02:00 PM 19/02/2021 |

*Signatures of those present:*

|  |  |
| --- | --- |
| **Supervisor:** |  |
| **Student: Matteo Bovino** |  |